SNS WIRE SCANNER USER GUIDE

by

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INTRODUCTION

The Spallation Neutron Source (SNS) is a large scientific-oriented facility being built in Tennessee USA that is comprised of a linear accelerator, storage ring and neutron scattering facilities. The SNS will be used to study the basic structures and properties of matter and materials using neutron scattering techniques. In the accelerator portion of the SNS facility, H^- particle beams are accelerated to 2.5 MeV in a radio-frequency quadripole (RFQ), to 87 MeV in a drift-tube linac (DTL), to 186 MeV in a coupled cavity linac (CCL), and finally to 1000 MeV in a super conducting linac (SCL).

Because of the high energy of accelerated particles, linac beam diagnostics are an essential subsystem of the accelerator. In the SNS linac, there are beam position monitors (BPM), wire scanners (WS), beam current monitors (BCM), beam loss monitors (BLM), and energy degrader/Faraday cups (ED/FC).

This document will describe the WS systems with an emphasis on the electronics and software and how to use the systems. More specific details of the mechanical actuators, bellows, selected wire types and analyses, and overview of the WS systems are found in other references. [1] This reference additionally contains numerous links to other published documentation about beam diagnostics.

In all, 52 WS systems will be required for the entire linac. The table below shows the number of WSs and their respective numbers and section in the linac.

Table 1. Quantities of WS systems per linac section.

	MEBT[2]	DTL	CCL	SCL
WS	5	5	10	32

The wire scanner actuators used in the MEBT, DTL, and CCL are based on linear actuators designed by LANL and purchased from Huntington Mechanical Laboratories, Inc. Each actuator fork has three 32-micron diameter carbon wires that can be biased to about ± 100 Vdc.

To date, the first five systems have been designed, manufactured and installed for use in the MEBT. The remaining WS systems are in the design phase and are based on the design of the MEBT WSs.

Under normal operation, the SNS linac will operate quasi-synchronous with the 60-Hz power grid at 60 pulses-per-second (PPS). The macro-pulse width will be up to 1 ms. Each macro pulse is comprised of mini-pulses about 690-ns wide at about 1-MHz repetition rate which depends on the exact storage-ring orbit time. The storage ring orbit time will vary

[1] Plum, M. A., et. al., "Beam Diagnostics in the SNS Linac," 2002 Beam Instrumentation Workshop, Brookhaven National Laboratory, May 6-9, 2002.

[2] Medium energy beam transport (MEBT), drift-tube linac (DTL), cavity-coupled linac (CCL), super-conducting linac (SCL)

somewhat in the range of 1.04 μs as a result of different orbit tunes. Each mini pulse is comprised of micro pulses at 425 MHz.

Because the H⁻ beam is too intense at full repetition rate and full macro-pulse width for the WS wires, when taking data, the macro pulse rate will be reduced to 1 to 6 Hz, and the macro-pulse width will be reduced to between 50 and 100 μs. Additionally, a ramp of about 30 μs will be included at the front-end of the pulse [3].

The wire scanners are based on a "networked system in a PC" model comprised of the major components in the figure below.

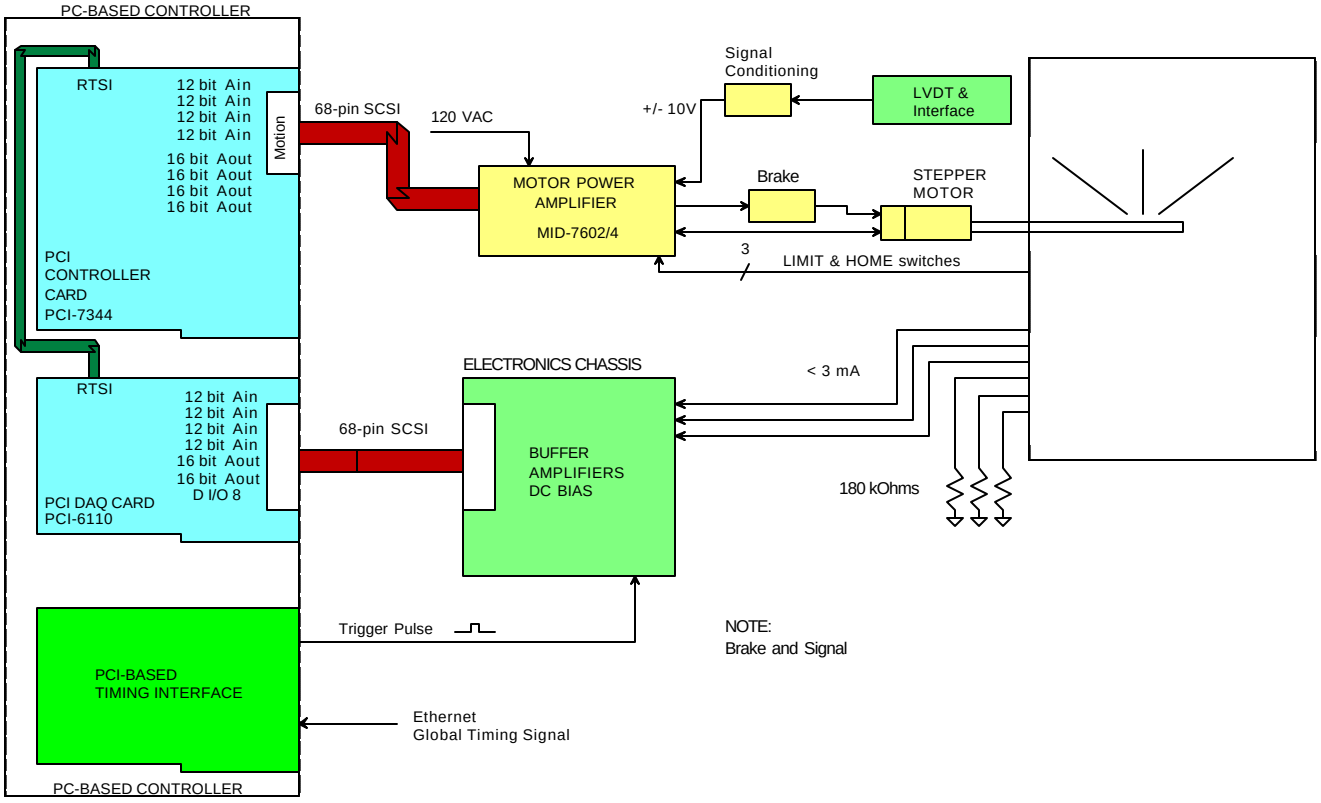

Figure 1. Block diagram of a wire scanner system.

Each WS system consists of an industrial personal computer (PC) running Windows 2000, LabVIEW and custom DLL software, an electronics chassis, a stepper-motor power amplifier, the linear actuator containing the beam-intercepting wires, and miscellaneous support electronics such as the LVDT and signal conditioning.

Inside the PC are one each of a digitizer and stepper-motor controller card from National Instruments, Inc. The digitizer uses 12-bit ADCs and can sample the signals from the three wires at up to 5 MSa/sec. The stepper-motor controller card sets and controls the position and movement of the wires by moving the actuator in and out of the beam.

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[3] A detailed timing diagram has been compiled by Coles Sibley of SNS for the entire accelerator.

The electronics chassis provides several functions including amplification and gain selection of the signals from the wires, a programmable high-voltage bias voltage, timing, built-in-test (BIT) and diagnostic capabilities.

The details of each of these components will be described in the following section.

The first five WS systems have been installed and successfully tested at LBNL where the injector and RFQ for the SNS linac were designed and first tested. The figure below is a picture of the WS actuators installed at Berkeley. The five actuators are visible as the gray rectangular boxes.

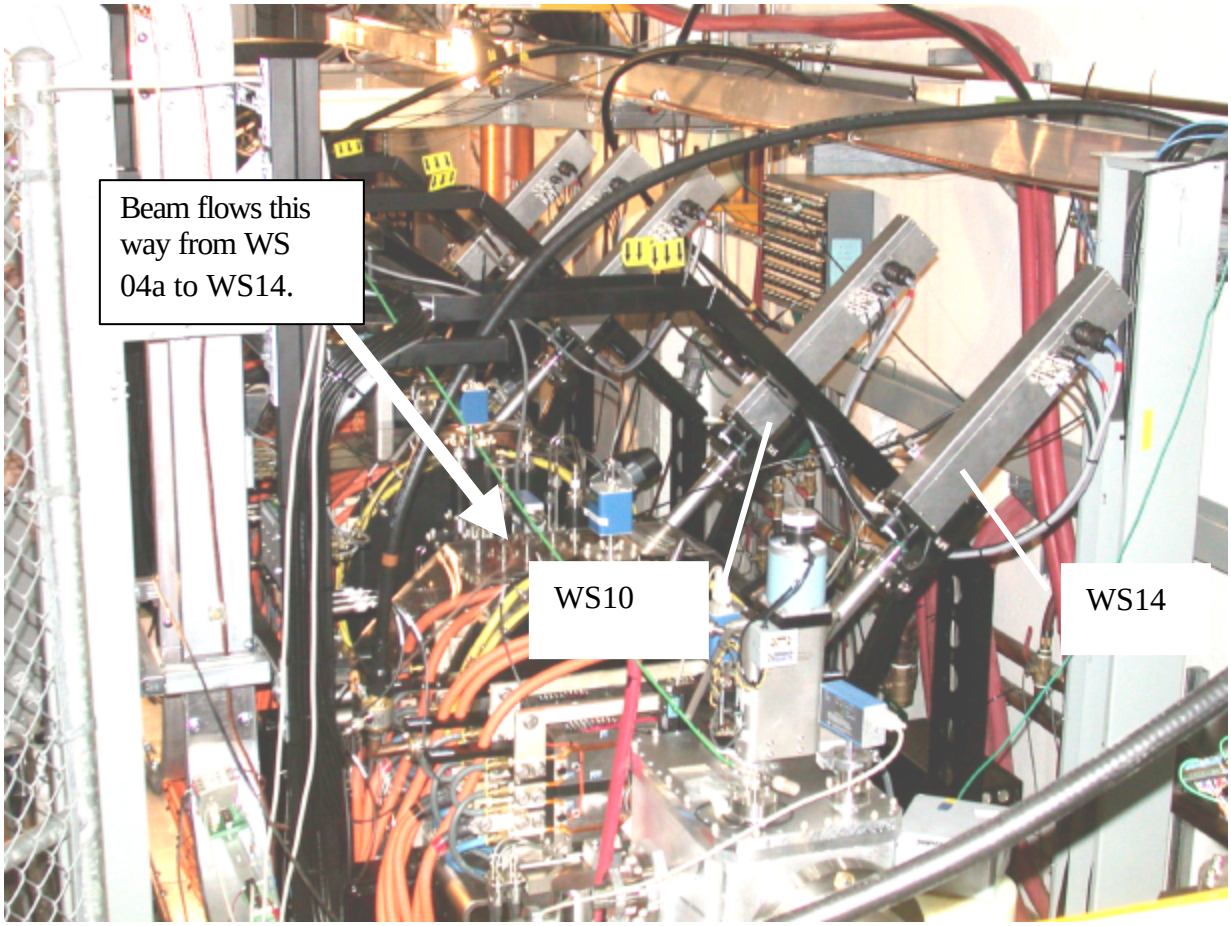

Figure 2. Picture of the WS actuators installed at Berkeley.

WS14 and WS10 are called out in the picture. The actuators for WS04a, 04b, and 07 are shown to the left of WS10. Each actuator is connected to the remote electronics chassis and stepper-motor driver by cables as shown.

The picture below shows the PCs, electronics chassis, and stepper-motor drivers installed in the racks at LBNL.

One system, consisting of the electronics chassis on top, the industrial PC, and the stepper-motor driver.

Four systems are shown in the figure. Each electronics chassis has front-panel connections for monitoring the timing signal and individual channel analog outputs. The fifth system is above and out of the picture.

Figure 3. Picture of the WS electronics installed at LBNL as part of the injector commissioning for SNS.

As each wire traverses the beam, it detects current and generates an output voltage waveform as a function of wire (X, Y, or Z) and actuator position. This information is useful in determining the size and characteristics of the beam at the specific WS location. The figure below shows a typical plot of the WS data.

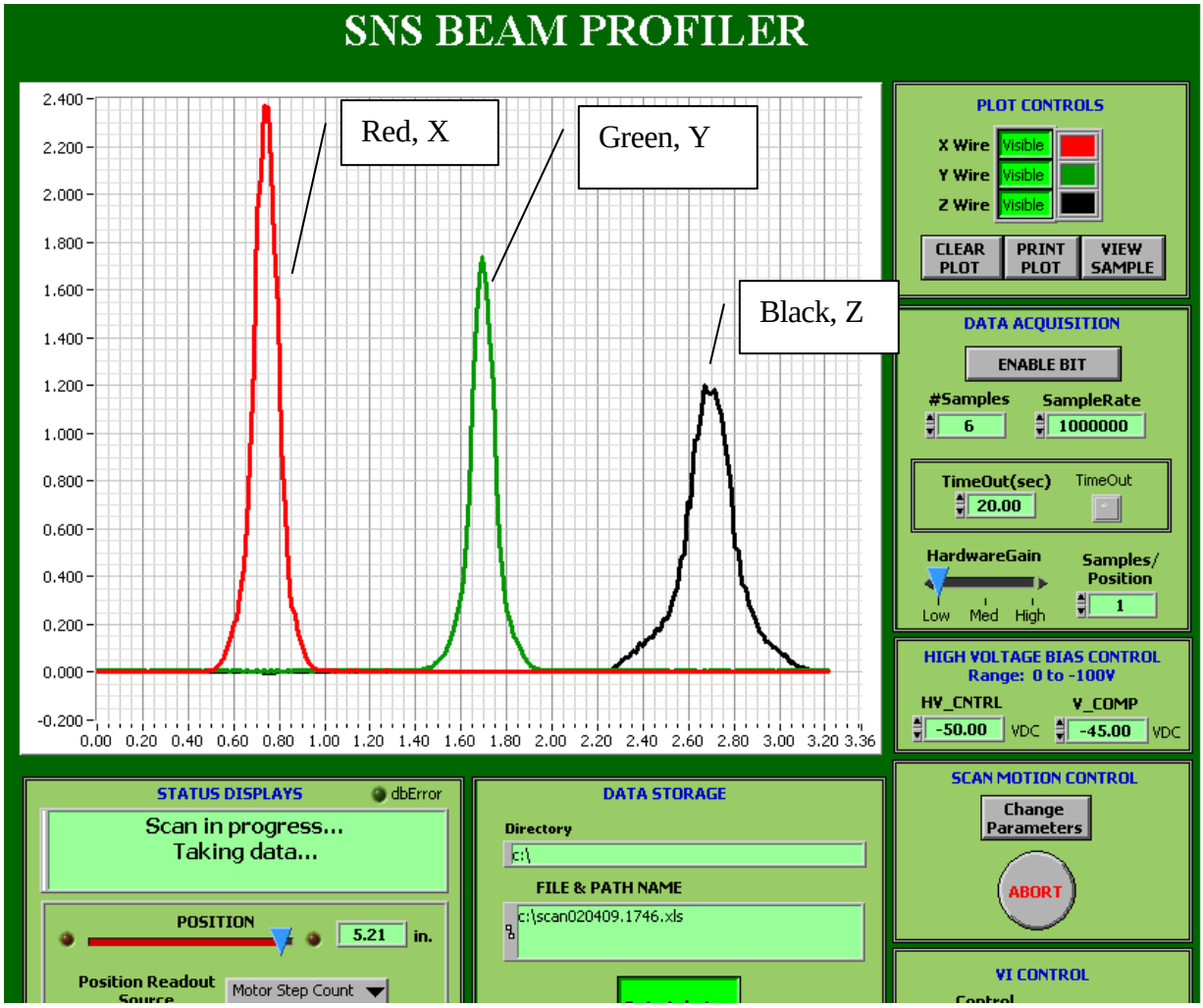

Figure 4. Graphic of a typical WS run. Software was done in National Instruments LabVIEW. Each of the three humps represents the current measured from each wire, X, Y, and Z. The scale is in volts and knowing the WS was set to "low" gain setting, can be converted to current at the wire. The x-axis is in inches.

This data was taken locally at the PC. The same information is sent via EPICS to the control system. Each WS system can be operated locally as each is a fully-functional networked-PC running LabVIEW with software links to Channel Access and the EPICS control environment. Each WS can be operated remotely via EPICS.

The remainder of this document will describe the WS systems in more detail, describe how to use the software and configure the hardware. Appendices list pertinent calibration data.

THEORY OF OPERATION

This section describes the theory of operation of the networked PC-based WS systems. The pertinent requirements and specifications are listed below.

SPECIFICATIONS

Table 2. Table showing the important wire scanner requirements and specifications.

ITEM	Value	Units
Macro pulse repetition rate	1-6	Hz
Macro pulse width	50 – 100	μs
Number of wire channels	3	
Channel sample rate	≤ 5.0	MSa/sec
Coupling to wires	AC	
Gain settings	3	~ 18 dB step
High-voltage bias	± 100	Vdc
Channel bandwidth	45	KHz, Low-pass
Peak beam current range[4]	5 - 60	mA
Max. input current (no damage)[5]	15	mA
Min. input current(noise floor)	< 0.1	μA
Electronics noise floor	< 1 LSB	< 4.88 mV any gain
Input signal polarity	Bipolar	
Max. input current, high gain[6]	30 ± 0.007	μA (10 Vdc FS)
Max. input current, medium gain	250 ± 0.06	μA (10 Vdc FS)
Max. input current, low gain	2400 ± 0.5	μA (10 Vdc FS)
Linearity	< 0.1	%
LVDT position resolution	± 0.24	Mill (2” stroke)
Wire position accuracy	0.25	mm

It should be noted that the macro pulse width and repetition rate are reduced from the nominal values of 60 Hz and 1 ms at those times when the WSs are in the beam and taking

[4] The peak beam current is different than the current on a wire as only a fraction of the beam current is intercepted and hence available at the electronics chassis for processing and analysis.
[5] The is the amount of current into the electronics of any one channel that will saturate the front-end OP AMPs.
[6] At this amount of current into any one channel, the output will be 10 Vdc. This is the scale factor for converting output voltage to input current as a function of selected gain.

data. The reduced values are shown above. Otherwise, the intensity of the full-power beam would destroy the wires.

WS SYSTEM BLOCK DIAGRAM

The block diagram of a wire scanner system is shown below. The system consists of an networked industrial personal computer (PC), electronics chassis, stepper-motor driver, and the actuator assembly and miscellaneous support devices such as the LVDT.

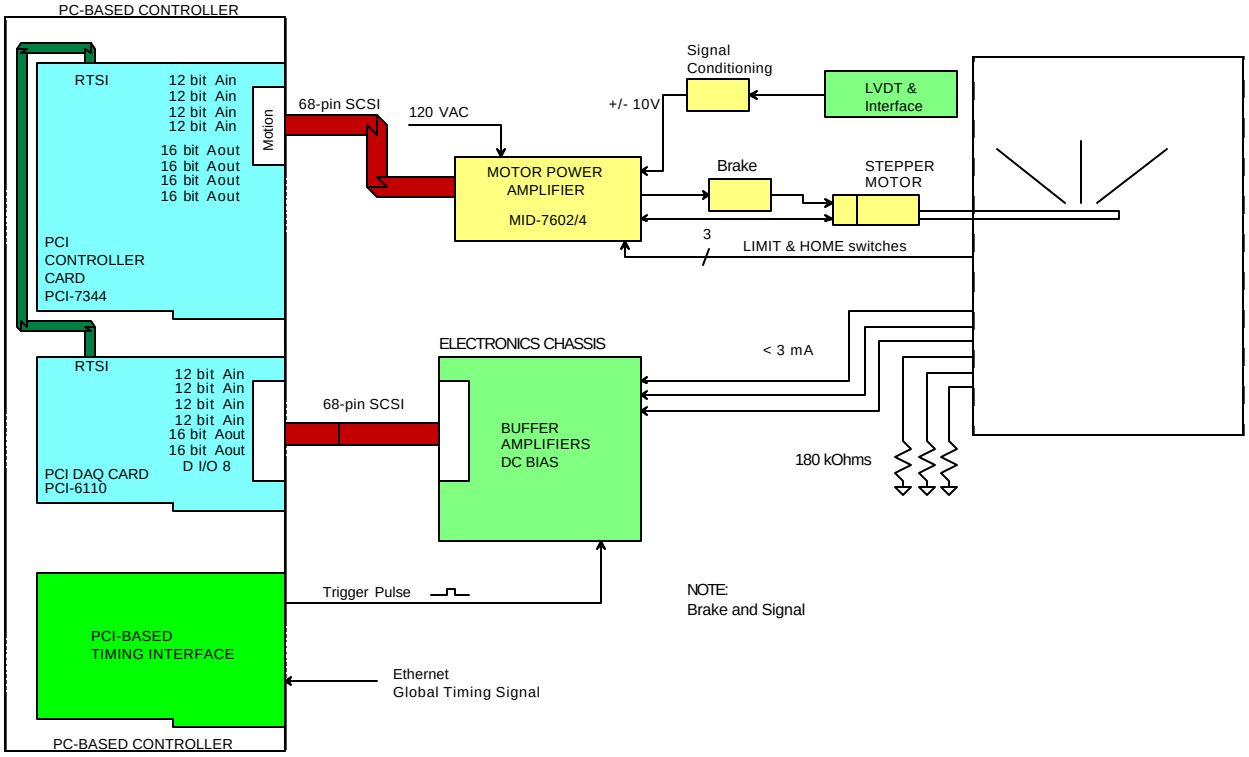

Figure 5. Simplified block diagram of a WS system.

The PC, electronics chassis, stepper-motor driver, and future LVDT interfaces are located in equipment racks some distance (at least 150 feet) from the actuator and beam line. Double-shielded coaxial cables (RG-223) carry current signals from the wires in the actuators to the electronics chassis. Because of the requirement to automatically detect a wire failure, and a requirement to voltage bias the wires, bias resistors of about 180 kΩ are installed on each of the wires at the actuator end. Each can be connected to earth ground. The bias and wire detection scheme is discussed in more detail in a later section.

A picture of the electronics racks is shown in figure 3. This picture was taken at the Berkeley installation and test of the injector and RFQ. Figure 2 shows the actuators also installed at Berkeley. The cabling to the actuators and the terminating resistors can be seen.

INDUSTRIAL PC

The industrial PC is a 4U high, 19" rack mount unit. It has an Intel motherboard, a 1-GHz processor and slots for up to five PCI plug-in boards. It is linked via Ethernet to the system-wide control system and is fully network compatible. Software also allows for complete remote control of the PC.

Control of the actuator position, hence the wire positions, and data taking is done using LabVIEW software. The LabVIEW software is written to include links to EPICS control system for remote control and monitoring. Additionally, each WS system can be operated locally.

Within each PC are two National Instruments PCI cards. One is the PCI-7344, stepper-motor control card; and the other is the PCI-6110 data acquisition cards. Provision has been made for a third card, a timing interface card that receives accelerator-wide timing information and outputs appropriate trigger information for data taking and movement in the WS system. Until the timing card is ready, trigger information has been input directly into the electronics chassis from the master timing system.

The PCI-7334 is a four channel stepper-motor control card. Upon initialization, it is loaded with acceleration, velocity and position settings and when commanded, it moves and positions the actuator at the required locations according to the LabVIEW run program. Signals from this card connect directly to the stepper-motor driver via a 68-pin SCSI cable. More information is available from National Instruments.

The PCI-6110 is a four channel, simultaneous, 5 MSa/sec, 12-bit data acquisition card. It also contains two 16-bit DAC outputs and eight bits of digital I/O. Additionally, each channel contains a programmable gain amplifier which can be adjusted under program control allowing fine tuning of signal amplification levels. This card is linked to the PCI-7334 controller card via an internal RTSI bus allowing synchronization between the two cards. More information is available at National Instruments.

In a normal operating scenario, the main LabVIEW program is started. It detects a software command to initiate and perform a beam scan. More detailed information about exactly how the system receives a signal from EPICS is available [7]. Upon receiving this signal, the PCI-7344 moves the actuator from a fully "out" position to a predefined beam- edge position. Upon arriving at the pre-set edge, the PCI-7334 then arms the PCI-6110 data acquisition card whereupon it waits for the next trigger edge. When it receives a trigger (via the electronics chassis), it samples data at pre-set rates and number of samples. It also has the ability to remain in the same position and average several trigger events before moving to the next position. After data taking is complete, the PCI-6110 informs the PCI-7344 which then moves the actuator to the next position and again arms the PCI-6110 and the cycle repeats. When the scan is complete, the actuator is returned to the fully "out" position. Data is made available during the scan to both the local PC display and to the EPICS control system via process variables.

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[7] M. Stettler and L. Day, Lansce-8, Los Alamos National Laboratory, Los Alamos, NM 87545

ELECTRONICS CHASSIS

The electronics chassis is a 1U-high 19-inch rack-mount unit that serves several functions: AC coupling of the wire signals; amplification and gain selection; low-pass filtering; high voltage bias; wire fault detection; and built-in-test (BIT) functions. Additionally, the timing/trigger signal is routed through this chassis to the PCI-6110 card.

A simple timing diagram is shown below. Part (a) shows a 60-Hz nominal beam mode waveform. The pulse width in this mode can be up to 1 ms. Part (b) shows a 6-Hz test mode waveform used for wire scans. The beam may operate at rates between one and six hertz for WS mode.

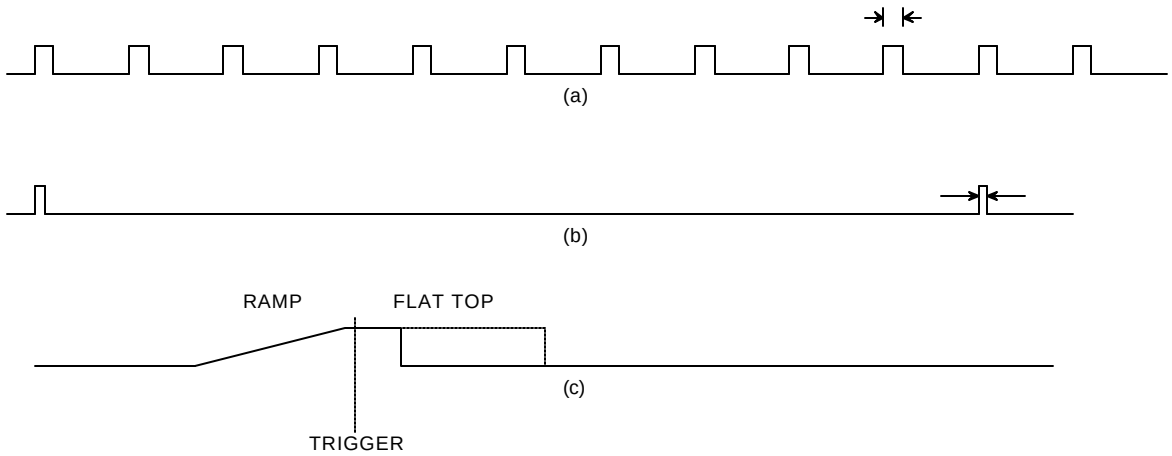

Figure 6. Timing diagram showing the nominal 60-Hz pulse repetition rate (a), and the pulses at 6 Hz (b). Part (c) is an expanded view of a test mode pulse showing a ramp, where triggering should occur after the ramp.

Part (c) is an expanded view of one of the pulses of part (b). It shows how the beam ramps up in 35-40 μs, has a flat top of about 10 to 65 μs and ends. The trigger should come about 7-8 μs before the end of pulse. This allows for settling in the preamplifier circuit and for at least six or seven data points to be taken before the end of the pulse. Total pulse width for wire scanner mode, including ramp time, is specified as between 50 and 100 μs.

The electronics chassis is shown in a simplified block diagram in figure 7. It shows three identical channels for the X, Y, and Z wire inputs, three identical high-voltage bias supplies, built-in-test circuitry, and connections to the host PCI-6110 data acquisition card.

Each channel has a separate high-voltage bias power supply capable of about ±100 Vdc. The high-voltage supplies are on a plug-in card so that positive (10 to 100 Vdc) or negative (-10 to –100 Vdc) supplies can be used by installing the appropriate type of card. Under normal operation, bias is applied to a wire by the high voltage power supply through a voltage dropping resistor/capacitor network of about 20 kΩ designated “LPF” in the figure. This voltage is measured by a voltage divider and applied to a voltage comparator. At the wire end, the 180 kΩ resistor acts as the other part of the voltage divider. If a wire were to break, the 180 kΩ resistor is removed from the circuit, and the voltage jumps to whatever the supply was set for. This jump will exceed the threshold on the comparator and generate a “wire failure” signal to the PC which in turn is relayed to the EPICS control system.

Wire signals coming into a channel are AC coupled, then a surge protector consisting of a 50-Ω resistor/capacitor network with a pole at about 10 MHz shunts the high-frequency components to ground (there will be substantial components at 425 MHz) and passes the remainder to the transimpedance amplifier. The gain can be selected as "low," "med," and "high" in 18-dB steps. The gain of all three channels are controlled together and are not independent. Diodes protect the input stages. The channel bandwidth is low-pass limited to 45 kHz instead of using an integrator as some other wire scanner designs use. This was a suitable compromise between adequate pulse response and low noise.

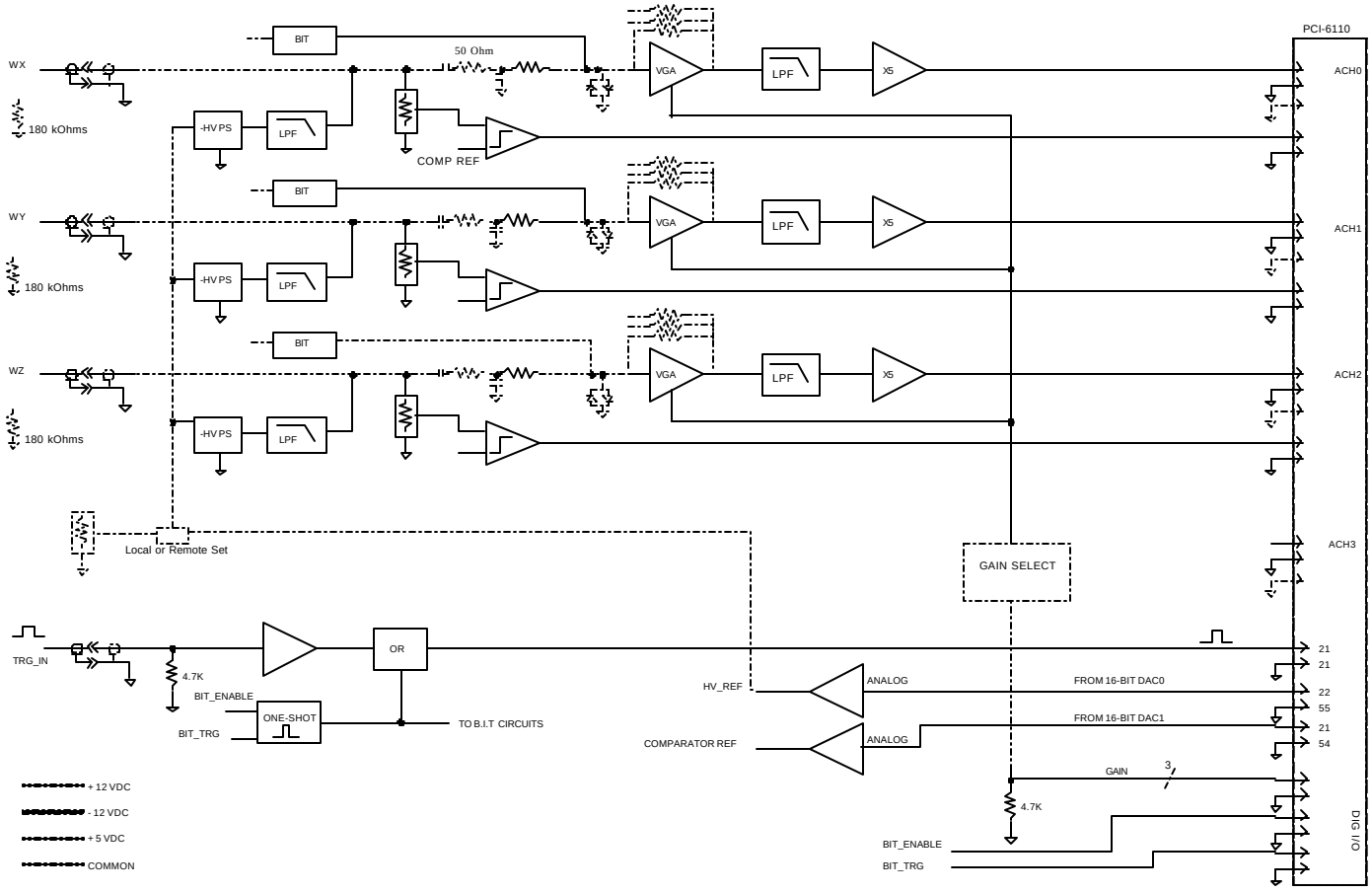

Figure 7. Simplified block diagram of the electronics chassis. Each of the three input channels, X, Y, and Z are identical. The channel gains are set together to one of three values. The bandwidth on a channel is set to 45 kHz with a three-pole low-pass filter.

The timing parameters, such as pulse width and repetition rate, are important because of the AC coupling and time constants of the preamplifier/gain circuits. As a result, the values of the AC coupling capacitors and input current-limiting resistors as well as the wire terminating resistors (180 kΩ) need to be carefully selected.

In the diagram below, current from the beam (modelled as a current source) is injected into both the 180 kΩ resistor and the 50-Ω cable connected to the electronics chassis. Nearly all goes in the cable. The resistor R1 in the electronics chassis shunts some away, the rest goes through AC-coupling capacitor C and through R3 to an OP AMP virtual ground. Ideally, the

time constant of C and R3 would be very large such that during a pulse there is minimal baseline shift. And ideally, the discharge time constant of C and R3 in parallel with R1 and R2 would be very short so that the circuit is completely discharged between pulses at the 6-Hz repetition rate. Ideally R1 would be very large to reduce lost current.

Given the constraints of a pulse width of up to 100 µs (this sets the C, R3 time constant), and a pulse repetition rate of up to six hertz (this sets the desired discharge time constant), values were selected using a linear programming model (Solver in Microsoft Excel) with all the constraints entered in the model. To provide adequate margin in the range of 10 time constants, the charge time-constant of R3 and C should be greater than 1 ms, and the discharge time constant less than 17 ms. The selected values are shown on the schematic.

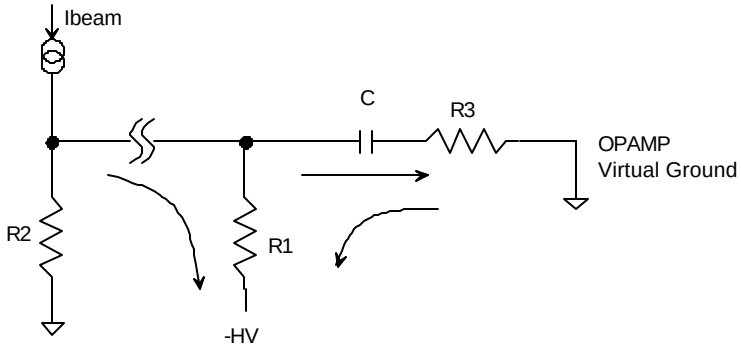

Figure 8. Simplified diagram showing the relationship between the circuit parameters and time constants for charging and discharging. Current from the beam is intercepted by the wire. Some is shunted by the 180-kOhm resistor, but most is transported to the electronics chassis. In side the chassis, resistor R1 shunts some to ground and the rest is AC-coupled to the OP AMP virtual ground. The time constant of C and R3 should be large compared to the width of the input pulse.

The built-in-test mode is particularly useful for testing the system from the amplifiers through the cabling and to the PCI-6110 and making sure it all works properly. The software selects BIT mode by enabling a bit in the electronics chassis which re-routes the trigger signal to a binary line from the PCI-6110. A trigger signal is then sent from the PCI-6110 causing the first of two 50-µs one-shot multi-vibrators to trigger. The first one generates a delay, and on the falling edge of its

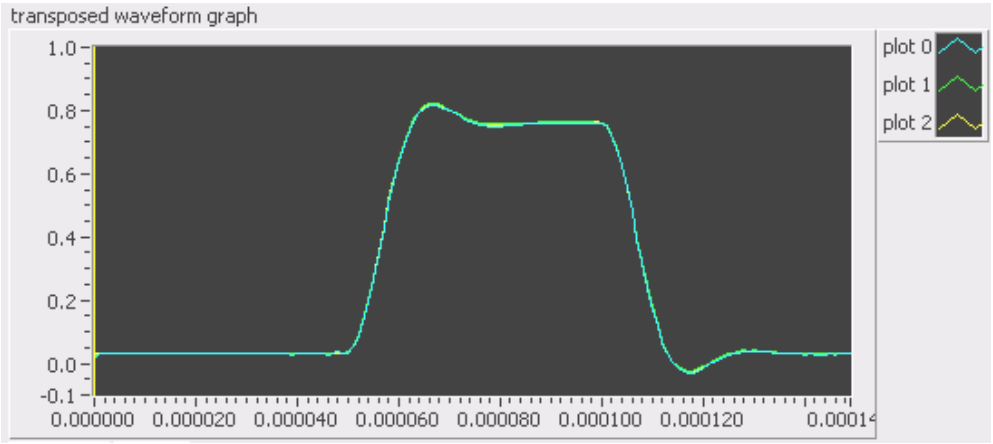

Figure 9. Screen capture of the digitized pulses from the electronics chassis when operating in BIT mode. Note that all three pulses overlay each other. This can be a quick test to verify proper operation of all channels. It can even show if the channels have the proper bandwidth.

output pulse, the second one fires generating a test signal that is coupled to the three channels via a 200-kΩ resistor. It shows all three channels. In this case, they overlap well which indicates excellent performance between the three of them. This is a useful diagnostic tool as any channel that isn't identical to the others will be obvious. Each channel is bandwidth limited to 45 kHz using a 3-pole Butterworth filter network. There is a slight overshoot to a square pulse input, and little overshoot with a ramp. The above figure shows the waveform when using a square pulse input. The pulse 50 μs and has some overshoot and undershoot. Data would be taken on the back porch of the flat top.

A photograph of the electronics chassis is shown below.

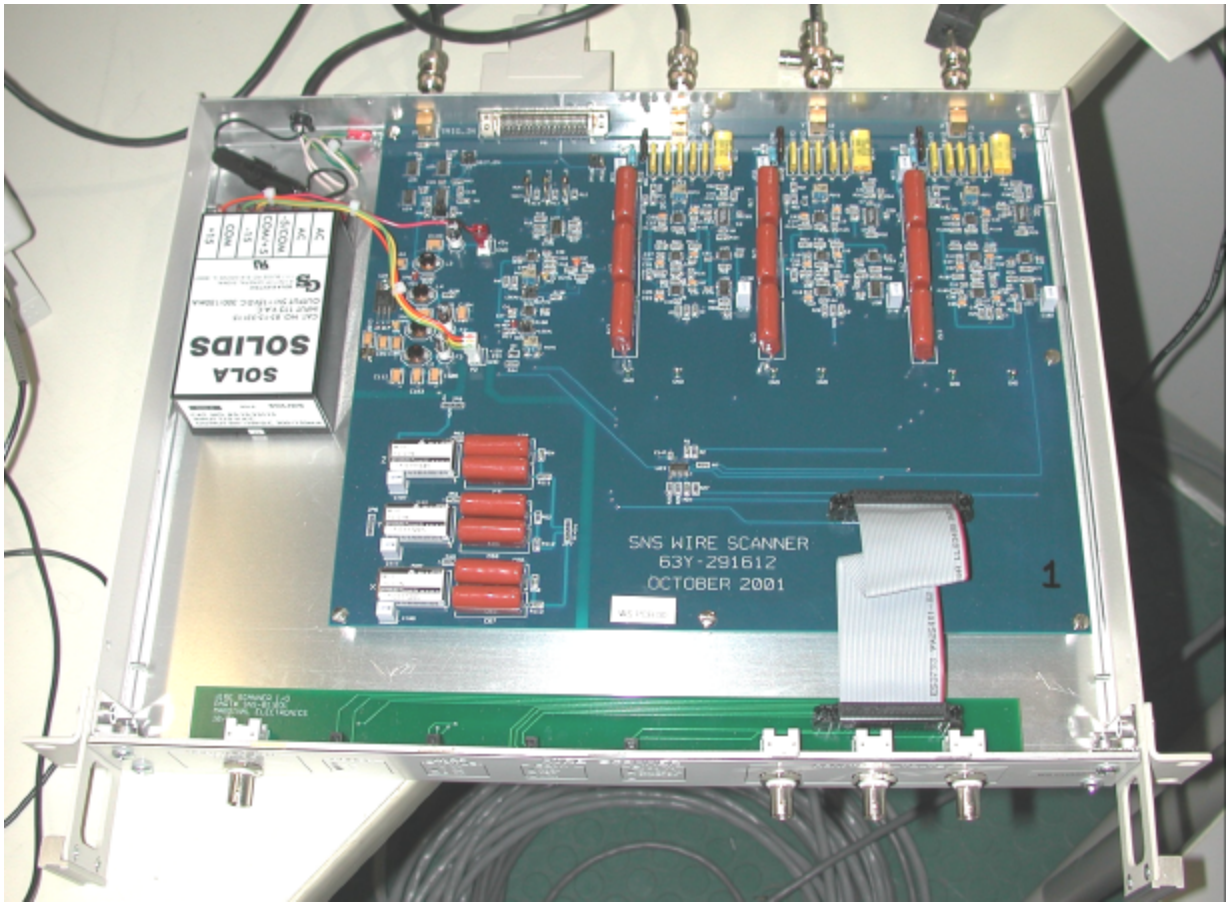

Figure 10. Photograph of the inside of the electronics chassis.

On the bottom left is the high-voltage bias section. On subsequent versions, these items are installed on a plug-in daughter card. The three input channels are visible on the top with the yellow AC coupling capacitors.

The high-voltage power supplies are from Matsusada Inc. and operate from +12 Vdc. They have a control voltage from 0 to 10 Vdc. A ribbon cable connects the main board to the front-panel board. A small printed circuit board mounted to the front panel provides a timing output, outputs for the channels, and LED indicators for gain and wire status as well as BIT status. The front panel is shown in the figure below.

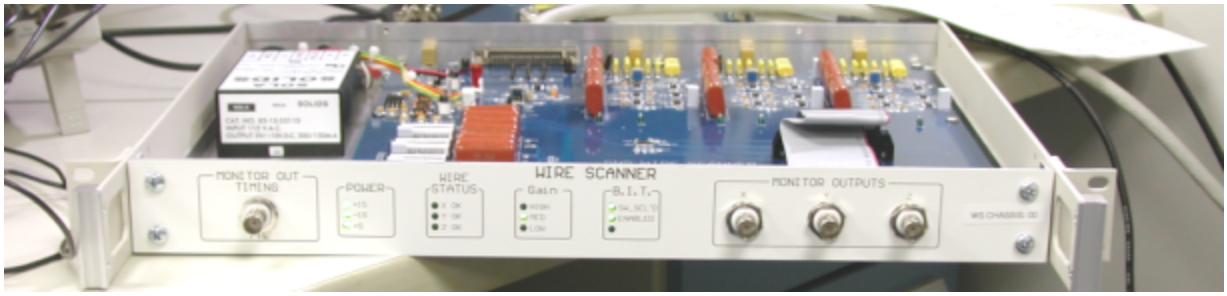

Figure 11. Picture of the front pane of the electronics chassis.

STEPPER DRIVER

The stepper-motor driver is a National Instruments MID-7602/4 unit. It operates using a PWM at 20 kHz. It allows for programmable peak and holding current. There is a plan to replace this unit with a linear-type that does not use a switching PWM architecture. The units delivered to Berkeley and first installed at the SNS facility are the PWM type.

A picture of the MID-7602 is shown below. On the front panel, there are numerous DIP switches which allow the setting of maximum output current and micro-stepping features. The switch settings are detailed on the top of the unit or in the unit's documentation. It connects to the PCI-7344 controller card via a 68-pin SCSI cable.

Figure 12. Picture of the stepper-motor driver, a National Instruments MID-7602/4. It uses a 20-kHz PWM architecture.

The terminal block to the upper-left provides a convenient connection interface. The power switch is on the back panel and an INHIBIT switch is on the front.

ACTUATOR

Because of the variation of the beam line, there are several mechanical variations of WS actuators. However, in each case, they are all based on a stepper-motor, ball-screw topology that allows accurate movement and positioning of the wires within the beam.

As a general overview, this section shows the actuator for the MEBT. More detailed information is available in the published literature regarding full mechanical specifications and features of all the WS mechanical variations.

The picture to the right shows a MEBT actuator mounted to a table with the cover off. This actuator was designed and fabricated by Brookhaven National Laboratory. The stepper motor is shown on the top of the housing connected to the ball screw. The beam-measuring wires are at the top mounted on the fork. Each wire has two isolated-ground BNC connectors. These are shown on the bottom.

The overall height of this unit is about 40 inches. The cover over the ball screw and internal wiring is removed in this picture.

A complete set of wiring diagrams and interconnections between the electronics chassis , the stepper-motor driver and each actuator has been completed and is available.[8]

A schematic of the isolated-BNC connectors is shown below. Using isolated BNC connectors allows for significant flexibility and grounding options to reduce or eliminate noise from the system. Short jumper strips were connected to the return tabs of each

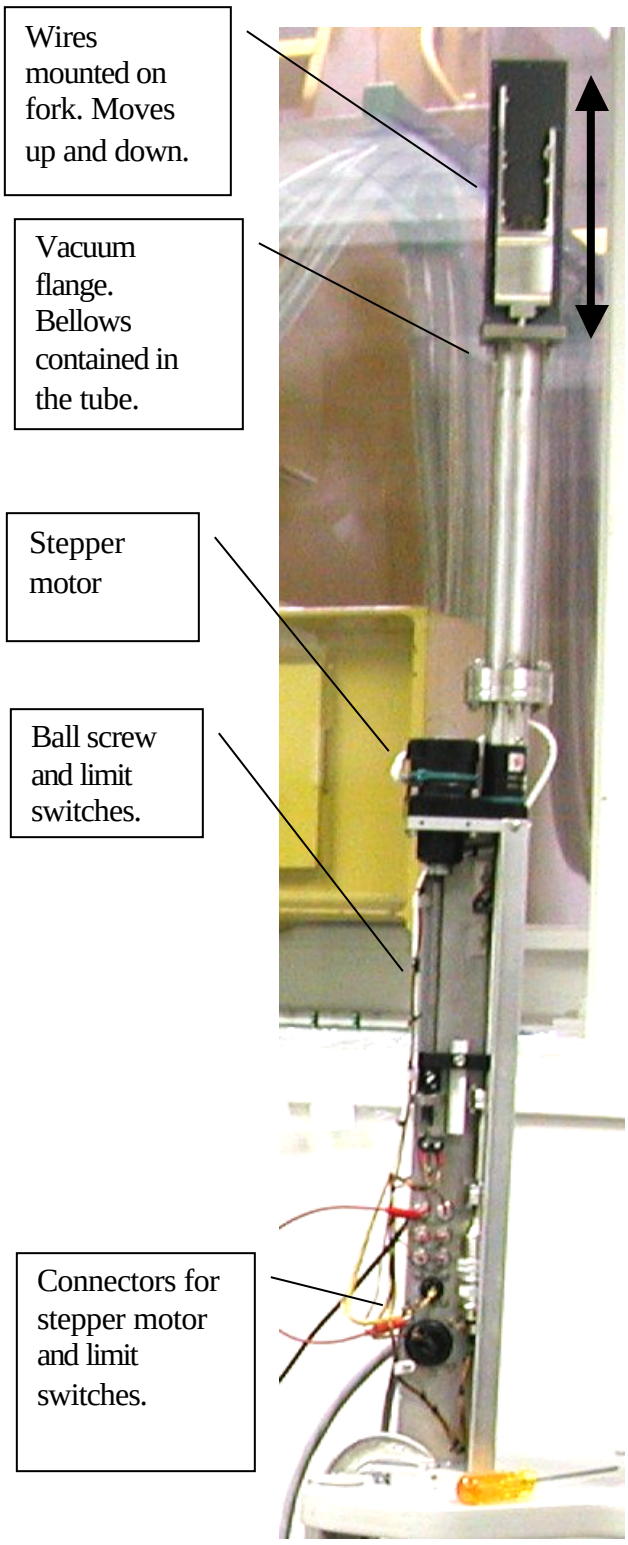

Figure 13. Picture of the actuator used for the MEBT.

[8] See Lansce-8, Los Alamos National Laboratory, Los Alamos, NM 87545.

connector pair to complete the circuit. It was found that maintaining a single point ground with each channel yielded the best noise performance. The signal-point ground for each circuit is at the electronics chassis. This was accomplished by not grounding the load resistors and not grounding the return tabs on each of the BNCs.

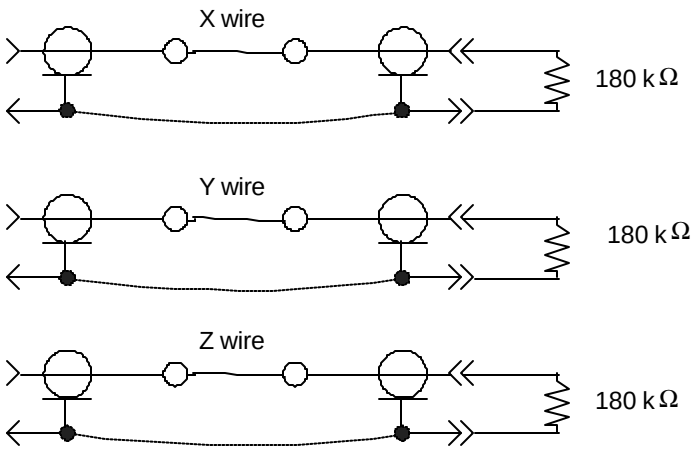

Figure 14. Schematic of the isolated-BNC connectors and how they are connected with the terminating 180-kohm resistors.

The dashed lines indicate the ground jumpers that were inserted to complete each circuit.

USING THE WIRE SCANNER SYSTEM

Each wire scanner system is based on a networked-PC model using both hardware and software subsystems. In order to obtain optimum results, each system needs to be properly calibrated. This section describes items such as how to calibrate the hardware and how to use the software screens to operate a system. We first start with a diagram of how the various software and hardware pieces are linked.

SOFTWARE

The figure below shows a simplified diagram of how the software and hardware are linked and interact.

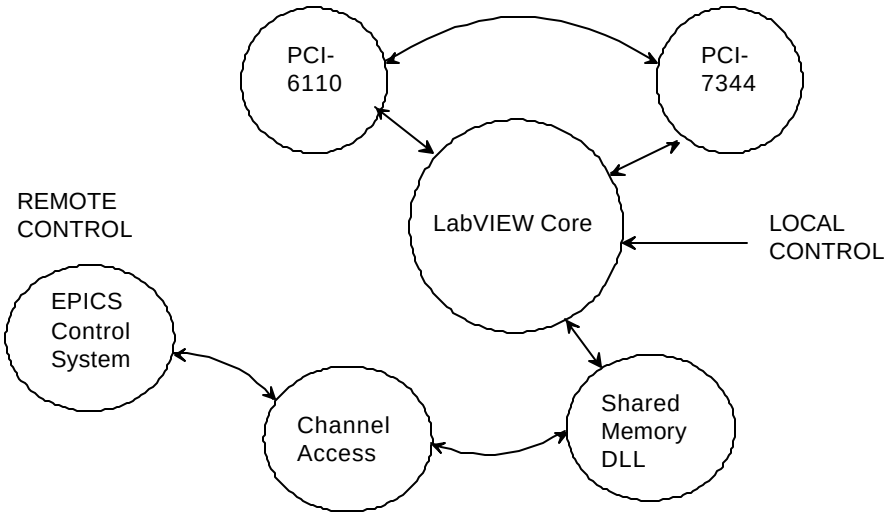

Figure 15. Simplified flow chart of the software interactions. The main program is a LabVIEW core with links via DLLs to the PCI cards. Additional links are made to EPICS.

The main program is written in LabVIEW and handles all interaction with the two PCI cards and serves as a GUI for a local operator at the PC. The hardware interaction is done via DLLs supplied by National Instruments. Additional links are included in the architecture via a shared-memory DLL that allows external systems like EPICS to send and receive data and information from the LabVIEW core[9].

Each WS system can be operated in LOCAL or REMOTE mode. In LOCAL mode, an operator interacts directly with the LabVIEW main GUI program. In REMOTE mode, a remote operator controls the system from an EPICS control screen. There is a third mode of control, though it is not the preferred method, where the PC can be controlled as if someone were sitting in front of it. This mode uses a "PC anywhere" type program.

[9] For more information, contact M. Stettler or L. Day, Lansce-8, LANL.

A detailed discussion of the software routines in the main LabVIEW program and DLLs is reserved for another text. This document is focused more on how to use the software and what it does.

Main LabVIEW Screen

The main LabVIEW GUI screen is shown in figure 4 and another example of it is shown below. It has eight main windows: the data viewer, plot controls, data acquisition , high-voltage bias, scan motion control, status displays, data storage, and VI control.

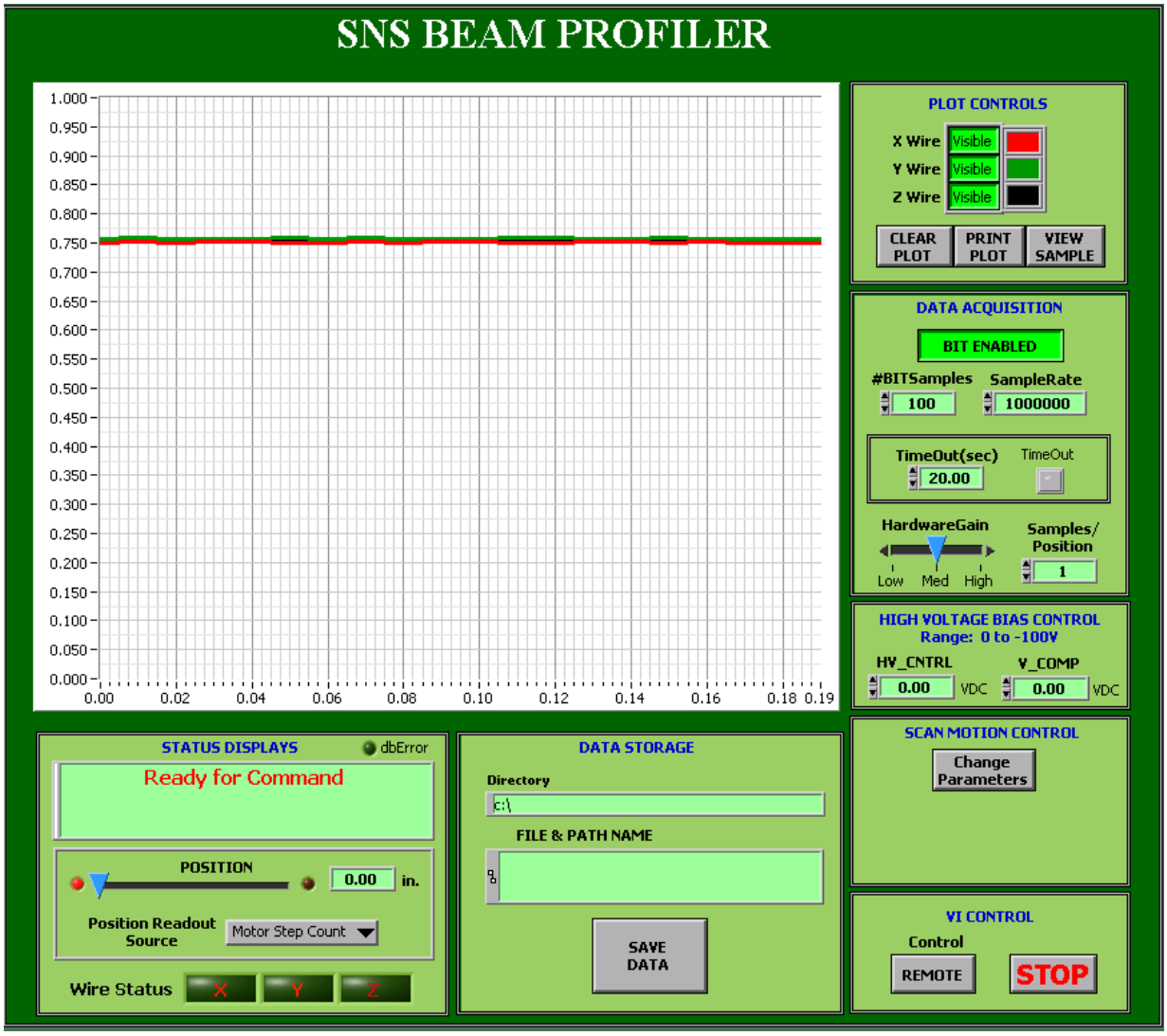

Figure 16. Graphic of the main LabVIEW user screen.

Data Viewer: Data from a scan is displayed in this window like that of figure 4. In the above figure, the WS has been operated in BIT mode and proper fixed values are displayed. The data are displayed left to right and are plotted in real time.

Plot Controls: These allow the operator to select which plots are visible and to view real-time samples from the ADCs for each channel.

Data Acquisition: Controls in this window select BIT mode or RUN mode, the number of BIT samples (or # of samples) and the ADC sample rate. When the BIT Enabled control is toggled, the number of samples control changes. Figure 4 shows the number of samples at 6 for a normal back-porch sample set. The sample rate is normally set to 1 MSa/sec but can be varied between 100 kHz and 5 MHz. The channel gain in the electronics chassis can be selected by moving the slider. Additionally, the number of samples to perform at each wire position can be selected. This allows averaging beam intensity on a pulse-to-pulse basis at each position.

High-Voltage Bias: The HV_CNTRL control is used to set the bias voltage on the wires. The V_COMP control sets the comparator voltage such that if a wire breaks, the bias voltage will jump, exceed the comparator voltage, and cause a Wire Status fault.

Scan Motion Control: This control is used to change set-up parameters of the motion controller and stepper motor. At start up, pre-set default values are loaded into the PCI-7344.

Status Displays: The position of the actuator is shown in real time in this window as well as the status of each of the wires.

Data Storage: The channel data can be stored after a scan by entering in the path and file name to be used for storage and pressing Save Data before initiating a run. This is a "local" feature and data are saved on the hard disk of the PC. External archiving and data storage features are available within EPICS.

VI Control: Pressing the "Control" button toggles between LOCAL and REMOTE control. At startup, it defaults to REMOTE operation. The STOP button terminates a scan and returns the system to its pre-scan condition.

Local Operation

The following steps should be followed to run a scan in LOCAL mode.

1. Press LOCAL if not already in LOCAL mode.
2. Set number of samples. Usually 6. The trigger signal needs to be set properly for a back-porch trigger.
3. Set sample rate. 1 MSa/sec is nominal. Range: 100 kHz to 5 MHz.
4. Set Samples/Position. Normally set to one.
5. Set electronics chassis gain, Low, Medium, or High. The setting will depend on how much beam is intercepted, and the beam current.
6. If needed, press the change parameters button and enter new values for the actuator step size, starting position, and stroke. The acceleration and velocity parameters of the motion control can also be adjusted.
7. Press the BEGIN BEAM SCAN button. A scan will start and the data from the wires will be displayed in the view window. The gains can be changed as the scan progresses.
8. If needed, the scan can be aborted by pressing the STOP button.

Remote Operation

When the software runs, it defaults to REMOTE operation. If however, it is in LOCAL mode, press the REMOTE/LOCAL button shown in figure 16 to change the state. With it in REMOTE mode, the indicators and data view window will still function, but control of scan variables will be done by the remote EPICS system. So, an operator can watch a scan take place and view the data but not change the settings.

Software BIT and Calibration

Each WS system includes built-in-test capabilities that allow the operator to quickly verify the proper functioning of major portions of each WS system. In BIT mode, a square pulse is injected immediately after the AC coupling capacitors in each electronics channel , X, Y, and Z, which is then routed through the system, digitized and displayed. An easy method of running BIT is to use the main screen shown in figure 16, then selecting BIT and VIEW sample. A sample screen is shown below.

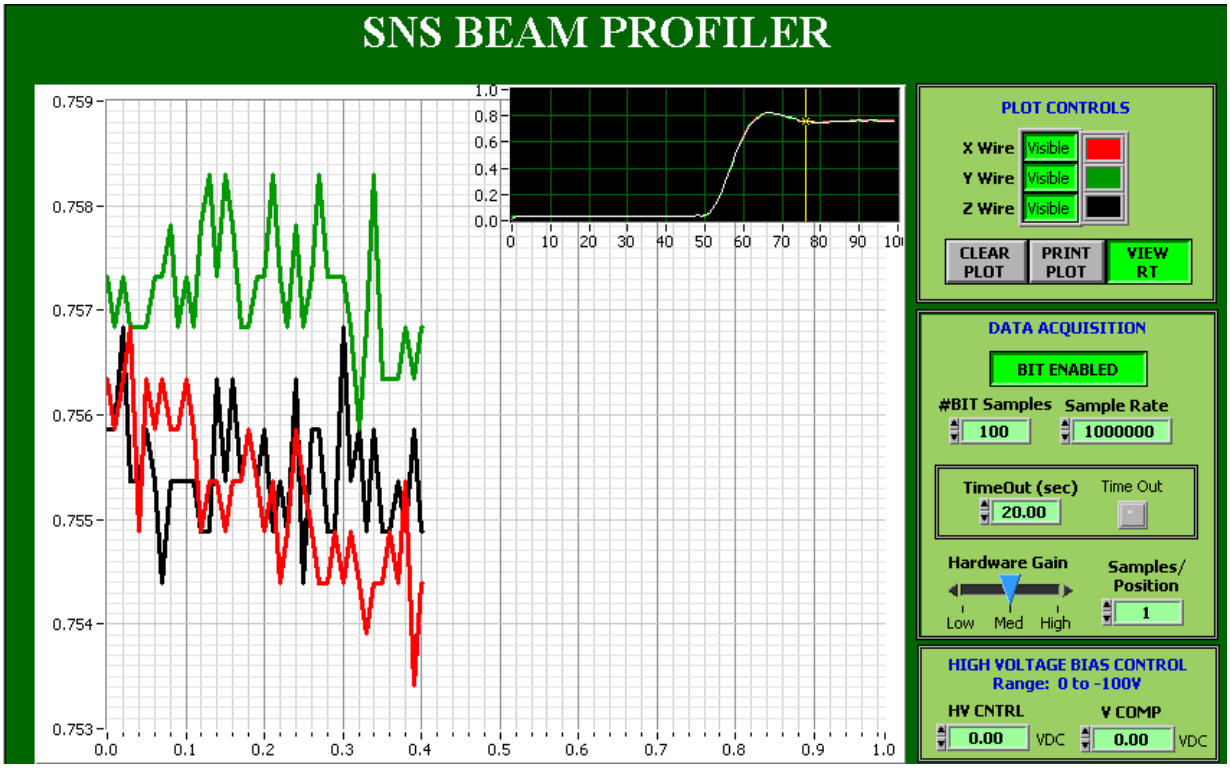

Figure 17. Screen shot of the main LabVIEW screen with the WS operating in BIT mode and the real-time view window open.

Notice in figure 17 that the VIEW RT button has been pressed which opens a window showing the sampled waveforms. A marker line indicates where triggering occurs and samples are taken.

In this mode, the actuator will move and act as though it were performing a real scan. However, the data from the wires will be replaced by known waveforms as shown in figure 17.

Another method exists to perform BIT without moving the actuator, but it requires two different LabVIEW programs and a little more user skill. The functions of these other programs have been integrated into the main LabVIEW program for ease of use.

CONFIGURATION

Each WS system must be connected to the other system components as shown in figure 5. On the electronics chassis circuit board ,there are several jumpers that can be configured.

Electronics Chassis

BIT_EN: This jumper is used for stand-alone testing of the circuit board. Normally it is set to the RUN position allowing remote software control.

One-Shot Delay: Jumper JP2. Options are Q for positive edge, and nQ or Q-bar for trailing/falling edge. There are two one-shots on the board that are used for BIT purposes. The first generates a 50-µs delay. Both its Q and nQ outputs are provided at JP2. The second one-shot is triggered on either the rising or falling edge of this first one-shot. The second one-shot generates a 50-µs pulse that can be applied to the three channels. Normally this jumper is set to nQ.

Trigger Output: Jumper P17. This jumper routes a trigger signal from the circuit board to the PCI-6110 on either PF10/Trig1 or PF11/Trig2. Normally set to PF10/Trig1.

Gain Selectors: Jumpers P8, 9, 10. Normally set to RUN. These can be used in manual mode to select the channel gains.

HV Set Input: Jumper JP1. This allows the HV power supplies to be set either by a remote voltage source on an on-board source. Normally it is set to REMOTE.

Threshold/Comparator Input: Jumper JP10. This allows the comparator thresholds to be set automatically by a scaled version of the HV set point, or from an external voltage source. Normally it is set to REMOTE.

Fuses: When powered, the LEDs for the +15, -15, and +5 should light. There is +12 V on the board for the HV supplies but there is no direct indicator for it.

Plug-in Card: Install the appropriate high-voltage plug-in card. There is one for positive voltage and one for negative. Each plug-in card must contain only positive or negative bricks with no mixing allowed.

PCI-Cards:

These cards should already be installed. If installing new cards, the drivers may need to be re-installed. When booting, Win2k will prompt for these drivers if it is the case. Sometimes they work loose during shipping and need to be re-seated.

CALIBRATION

Each WS system arrives “factory” calibrated. However, there may be times when a re-check or re-calibration is required. The major components that may require re-calibration are

the electronics chassis, the data acquisition card, and the motion control card. Some of the calibration must be done manually, and some can be performed using supplied LabVIEW software. The following is brief description of how to perform these calibrations.

Electronics Chassis

Items that can be calibrated in the electronics chassis are the channel offset voltage and the high-voltage output versus set point.

Channel Offset Voltage: This adjustment removes any DC offset as a result of the OP AMP stages in a channel.

- Install short or 50-Ω terminator on X, Y, Z inputs on rear panel.
- Allow the circuit board to warm up for at least 10 minutes.
- Preferably set the HV to zero output though not absolutely necessary.
- Ensure BIT mode is DISABLED. An easy way to do this is to remove the jumper from the BIT_EN jumper block. Don't forget to put it back when finished.
- Select high gain. Position the jumper on SEL_D to TEST. SEL_C and SEL_B should be at the RUN position. This adjusts the gain of all three channels together.
- Measure voltage at front panel X-Monitor output (alternatively, measure at U7-6) and adjust POT1 near U12 for minimum DC voltage.
- Measure voltage at front panel Y-monitor output (alternatively, measure at U9-6) and adjust POT2 near U14 for minimum DC voltage.
- Measure voltage at front panel Z-monitor output (alternatively, measure at U8-6) and adjust POT3 near U13 for minimum DC voltage.
- Replace SEL_D jumper to RUN position.
- Replace BIT_EN jumper to RUN.

PCI-6110

This card comes pre configured. For calibration, see National Instruments documentation.

PCI-7344

This card comes pre configured. For calibration, see National Instruments documentation.

APPENDIX A

Although every attempt has been made to make each wire scanner system identical to the others, slight discrepancies exist such as in the gains and offsets of the analog-to-digital converters (ADCs), the transfer functions of the high-voltage power supplies, the channel gain values, and other systematic errors. As a result of these errors, each system has been measured and has an individual set of calibration data.

GAIN CALIBRATION DATA

The channel gains track closely enough to be considered identical.

WIRE BIAS CALIBRATION DATA

These data are used to calculate the SLOPE and OFFSET coefficients that are used when setting the bias on the wire for the negative high-voltage bias supplies:

	WS04a			WS04b			WS07			WS10			WS14		
Set Point	B	D	F	B	D	F	B	D	F	B	D	F	B	D	F
0															
-10															
-20	-11.70						-11.69	-11.68	-11.62	-11.75	-11.80	-11.61	-11.63	-11.64	-11.59
-30	-21.00	-21.00	-21.00												
-40							-30.78	-30.76	-30.74	-30.80	-30.90	-30.50	-30.48	-30.59	-30.50
-50	-40.30	-40.32	-40.50												
-60							-50.18	-50.16	-50.18	-50.30	-50.40	-49.70	-49.67	-49.87	-49.73
-70															
-75	-64.40	-64.50	-64.82												
-80							-69.40	-69.50	-69.50	-69.70	-69.80	-68.90	-68.80	-69.00	-68.90
-90															
-95	-83.60	-83.60	-81.10												
-100							-88.70	-88.80	-88.70	-89.00	-89.00	-87.90	-87.80	-88.20	-87.90
slope	0.960	0.964	0.931	#DIV/0!	#DIV/0!	#DIV/0!	0.963	0.965	0.965	0.967	0.967	0.9549	0.9533	0.95765	0.9551
intercept	7.67	7.87	6.32	#DIV/0!	#DIV/0!	#DIV/0!	7.64	7.71	7.73	7.71	7.61	7.57	7.52	7.60	7.58
avg. slope	0.952			0.957			0.964			0.963			0.955		
avg. intercept	7.29			7.45			7.69			7.63			7.57		

Figure 18. Graphic showing the data used to calculate individual system SLOPE and OFFSET values used for wire bias voltage.

The left column lists the set points, the other columns show the measured wire voltages. The slope and intercept values are calculated by Excel using a least-squares-fit of the data using the form

$$y = mx + b$$

where,

m = slope
b = intercept
and x = Set Point

These values were originally entered into data files which the LabVIEW program read and used to provide the correct output voltage as commanded. The fit values take into account the

linear errors of the high-voltage power supplies and the effects of the voltage divider. However, a simpler, easier method has been found to calibrate the high-voltage output to the wires.

IMPROVED METHOD

The first version of electronics chassis used only negative bias high-voltage supplies. A subsequent modification has added a plug-in daughter card containing either three positive or negative power supplies.

Rather than taking measurements and calculating linear regression slope and offset coefficients to be used in setting the wire bias voltage, a simpler method is to set the desired wire voltage using the V_COMP control, and then adjust the wire bias voltage, HV_CNTRL until the WIRE STATUS indicators light. This has proven to yield results within one volt of the expected value and close enough for these measurements.[10]

[10] Notes from W. Christensen.

APPENDIX B

WIRE MEASUREMENT METHOD

The following is a brief explanation of how three wires are used to measure and determine the profile of a particle beam.

In the diagram below, the beam is represented as a horizontally oriented ellipsoid. As the wires cut through the beam, because of their different angles, each measures a different aspect of the beam profile. Additionally, the displayed data will have a position offset and amplitude and width variations.

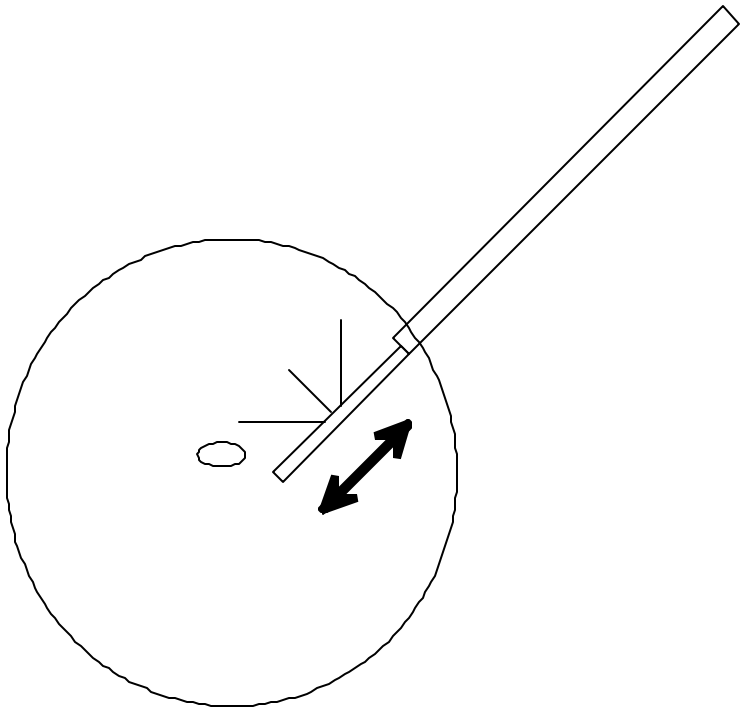

Figure 19. Simplified diagram showing the relationship between the three wires and the beam. The beam is shown in the middle as an ellipsoid. The wires intercept the beam and measure its profile.

In the figure, the bottom wire is X, the first to intercept the beam, and would see a relatively narrow beam with greater peak amplitude. The middle wire, Y, would see and measure a slightly larger beam with less amplitude. And finally, the last wire, Z, would measure a still wider beam and with reduced amplitude.

This concept is loosely illustrated by data taken at Berkeley and shown below in the following figure.

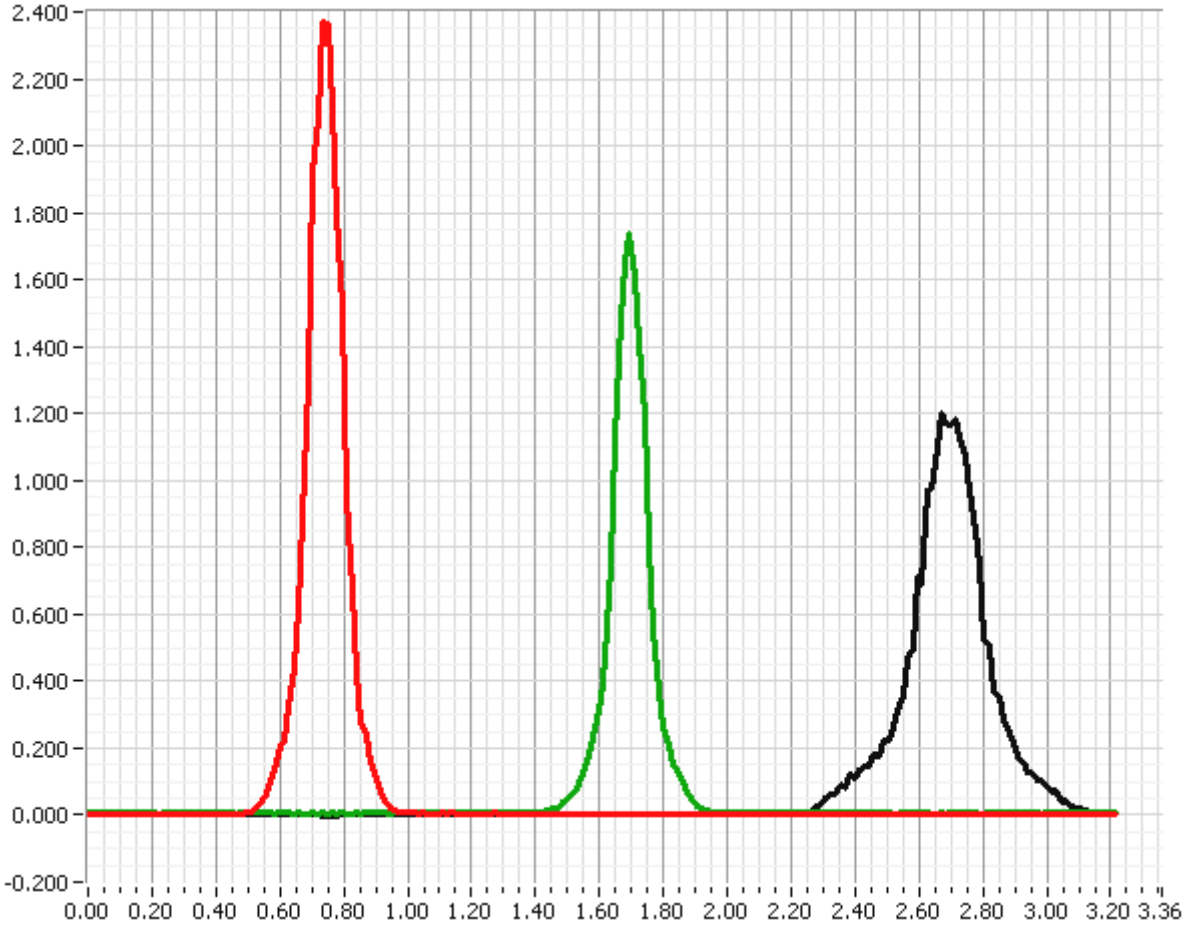

Figure 20. Data taken on WS14 at Berkeley showing amplitude and width variations from the three wires. Left scale is volts and bottom-scale is in inches. The channel gain was set to low.

As shown in the figure, each wire intercepts the beam at a different actuator position, and depending on the beam shape, generates a different profile as it sweeps through.